Abstracts

High Sensitivity InP-Based Monolithically Integrated Pin-HEMT Receiver-OEIC's for 10 Gb/s

W. Kuebart, J.-H. Reemtsma, D. Kaiser, H. Grosskopf, F. Besca, G. Luz, W. Korber and I. Gyuro. "High Sensitivity InP-Based Monolithically Integrated Pin-HEMT Receiver-OEIC's for 10 Gb/s." 1995 Transactions on Microwave Theory and Techniques 43.9 (Sep. 1995, Part II [T-MTT] (Special Issue on Microwave and Millimeter Wave Photonics)): 2334-2341.

InP-based pin-HEMT receiver-OEIC's with different circuit layouts for bit rates up to 10 Gb/s are simulated, realized and characterized. The circuits under investigation are a high impedance amplifier, a common-gate circuit, and a transimpedance-cascode circuit. The high frequency behavior of all circuits is compared by means of on wafer-characterization. All circuits show a bandwidth of more than 5 GHz, the transimpedance circuit has the highest responsivity (12.9 dB A/W) and a very low average noise current of 11.5 pA/spl radic/HZ when assembled in a module. The receiver sensitivity of the transimpedance circuit in the module is measured to be as high as -19.2 dBm.

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